IDS Form PTO/SB/08: Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	10/086,549
Filing Date	3/4/02
First Named Inventor	YUTAKA ARIMA
Art Unit	2121
Examiner Name	[illegible]
Attorney Docket Number	08372.0007

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

Note: Copies of the U.S. Patent Documents are not Required in IDS filed after October 21, 2004

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
H		YUTAKA ARIMA, "Higher Integration of Neural Network with Learning Function," Study of Associative Memory Analog Neural Network LSI with Learning Function (January 1998).	√
H		"Chaos and Associative Memory," Computer Today (July 1999).	√
H		YUTAKA ARIMA, et al., "A Self Learning Neural Network Chip with 125 Neurons and 10K Self-Organization Synapses," 26 IEEE Journal of Solid-State Circuits 607 (April 1991).	
H		YUTAKA ARIMA, et al., "A 336-Neuron, 28K-Synapse, Self-Learning Neural Network Chip with Branch-Neuron-Unit Architecture," 26 IEEE Journal of Solid-State Circuits 1637 (November 1991).	
H		YUTAKA ARIMA, et al., "A Refreshable Analog VLSI Neural Network Chip with 400 Neurons and 40K Synapses," 27 IEEE Journal of Solid-State Circuits 1854 (December 1992).	

Examiner Signature	[signature]	Date Considered	1/13/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO Notes regarding this form:

[1] Applicant's unique citation designation number (optional).
[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.
[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).
[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.
[6] Applicant is to place a check mark here if English language Translation is attached.